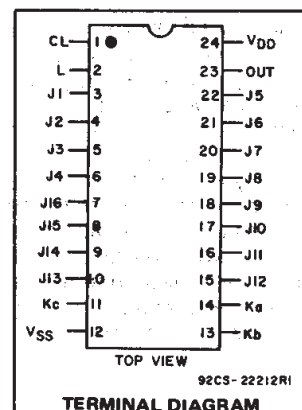# CD4059A Types

CMOS Programmable Divide-by-"N" Counter

Standard "A"-Series Types (3-to-15-Volt Rating)

■ CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode Select Inputs Ka, Kb, and

Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

CL	1	24	VDD
L	2	23	OUT
J1	3	22	J5
J2	4	21	J6
J3	5	20	J7
J4	6	19	J8
J16	7	18	J9
J15	8	17	J10
J14	9	16	J11
J13	10	15	J12
Kc	11	14	Ka
VSS	12	13	Kb

TOP VIEW

92CS-22212RI

TERMINAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) .... −0.5V to +15V

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −55°C to +100°C 500mW

For T_A = +100°C to +125°C... Derate Linearly to 100mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	−	3	12	V
Clock Pulse Width	5	200	−	ns
	10	100	−	
Clock Input Frequency	5	−	1.5	MHz
	10	−	3	
Clock Input Rise and Fall Time	5	−	15	µs
	10	−	5	

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°	−40°	+85°	+125°	+25° Min.	+25° Typ.	+25° Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	−	0.02	10	µA
			10	20	20	200	400	−	0.02	20	
			15	−	−	−	−	−	−	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				−	0	0.05	V
		0,10	10	0.05				−	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	−	
		0,10	10	9.95				9.95	10	−	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	−	V
			10	3				3	4.5	−	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	−	
			10	3				3	4.5	−	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High,	0.5		5	1							

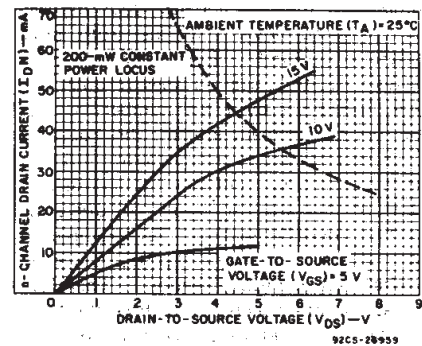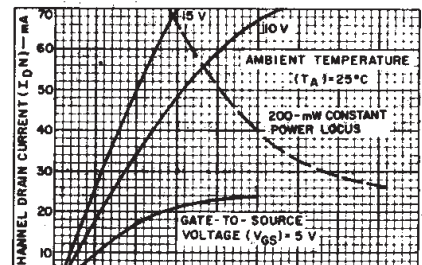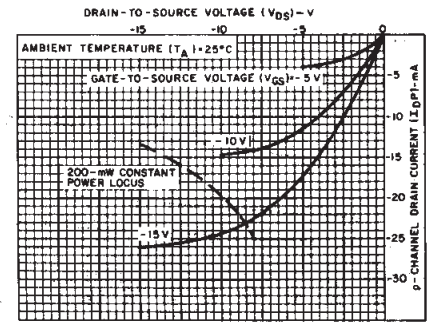*Fig.2 — Minimum output n-channel drain characteristics.*

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^O C$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	CONDI-TIONS V_{DD} (V)	LIMITS ALL PACKAGES			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time; t_{PHL}, t_{PLH}	5	—	180	360	ns
	10	—	90	180	
Transition Time:					
t_{THL}	5	—	35	70	ns
	10	—	20	40	
t_{TLH}	5	—	100	200	
	10	—	50	100	

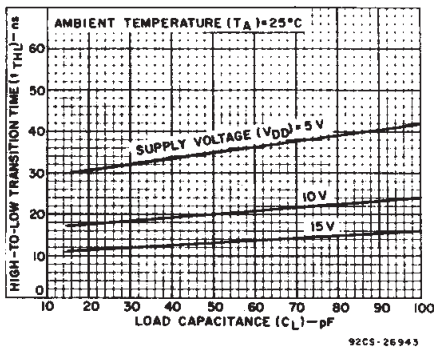Fig.6 — Typical output p-channel drain characteristics.

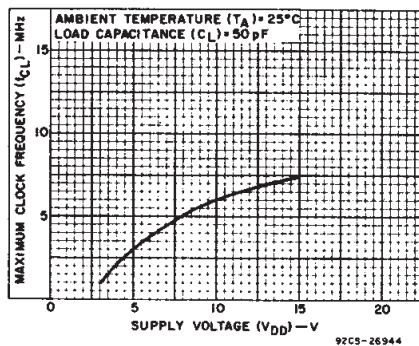Fig.10 — Typical high-to-low transition time vs. load capacitance.

Fig.11 — Typical max. clock frequency vs. supply voltage.

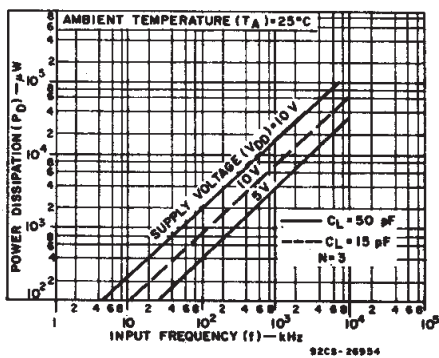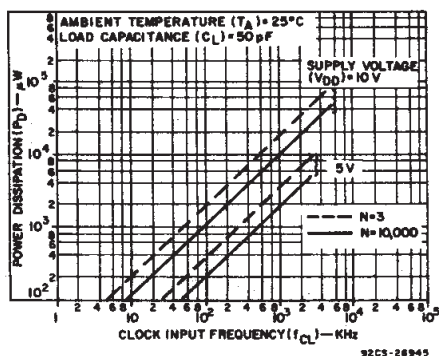Fig.12 — Typical power dissipation vs. input frequency.

Fig.13 — Typical power dissipation vs. clock input frequency.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Divides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Divides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	—	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			—	—

X = Don't Care

▲ J1 = Least significant bit.
  J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "0" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts. See Fig. 21 for a suggested external preset circuit.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

$$N = [MODE^*] \quad [1000 \times \text{Decade 5 Preset} + 100X \text{ Decade 4} \tag{1}$$

Preset + 10X Decade 3 Preset + 1X Decade 2 Preset] + Decade 1   Preset

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \tag{2}$$

Examples:

A)   N = 8479, Mode = 5

MODE SELECT = 5

      1695 + 4 ← Preset Values
   5 | 8479
Mode   N

Ka Kb Kc
 1   0   1

PROGRAM JAM INPUTS (BCD)

4				1	5				9				6			
J1	J2	J3	J4		J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1		1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

B)   N = 12382, Mode = 8

MODE SELECT = 8

      1547 + 6
   8 | 12382

Ka Kb Kc
 0   0   1

PROGRAM JAM INPUTS

6				1				7				4				5			
J1	J2	J3	J4		J5	J6	J7	J8		J9	J10	J11	J12		J13	J14	J15	J16	
0	1	1	1		1	1	1	0		0	0	1	0		1	0	1	0	

To verify:

$N = 8 (1000 \times 1 + 100 \times 5 + 10 \times 4 + 1 \times 7) + 6$

$N = 12382$

MODE SELECT = 10

C)   N = 8479, Mode = 10

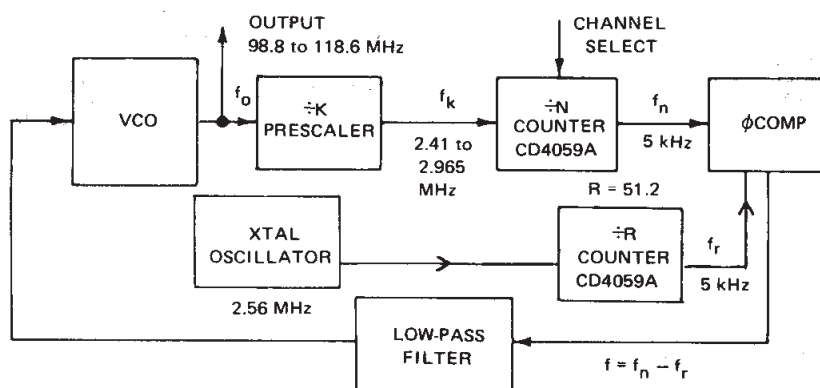$$\begin{array}{r} 0847 + 9 \\ \hline 10\,\lfloor 8479 \end{array}$$

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

$N = 10 (1000 \times 0 + 100 \times 8 + 10 \times 4 + 1 \times 7) + 9$

$N = 8479$

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER

1) Calculating Min & Max "N" Values :

Output Freq. Range (f_0) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_c) = 200 kHz

Division Factor (k) = 40

Reference Freq. $(fr) = \dfrac{f_c}{k} = \dfrac{200}{40}$ kHz = 5 kHz

$f_k = \dfrac{f_0}{40}$: $f_k Max. = \dfrac{118.6\ MHz}{40} = 2.965\ MHz$; $f_k Min = \dfrac{98.8\ MHz}{40} = 2.47\ MHz$

$\therefore\ N = \dfrac{f_0}{f_c}$

$N_{Max} = \dfrac{118.6\ MHz}{200\ kHz} = 593$ $N_{Min} = \dfrac{98.8\ MHz}{200\ kHz} = 494$ $R = \dfrac{2.56\ MHz}{5\ kHz} = 512$

"CASCADING" VIA OTHER COUNTERS

Fig. 14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

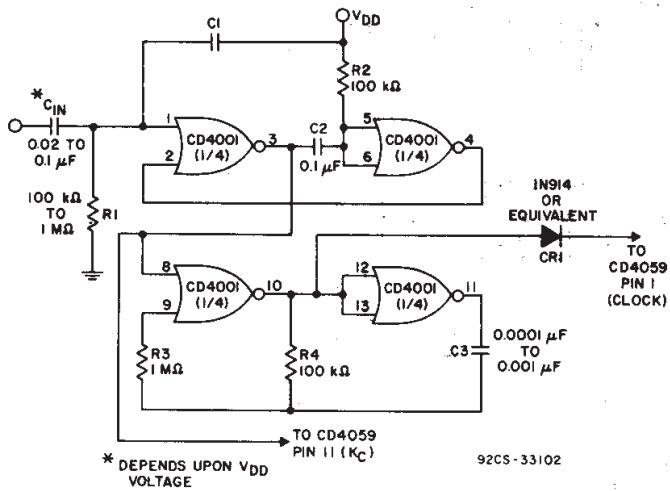2) ÷ N Counter Configuration for UHF — 220 to 400 MHz
Channel Spacing: 50 kHz or 25 kHz
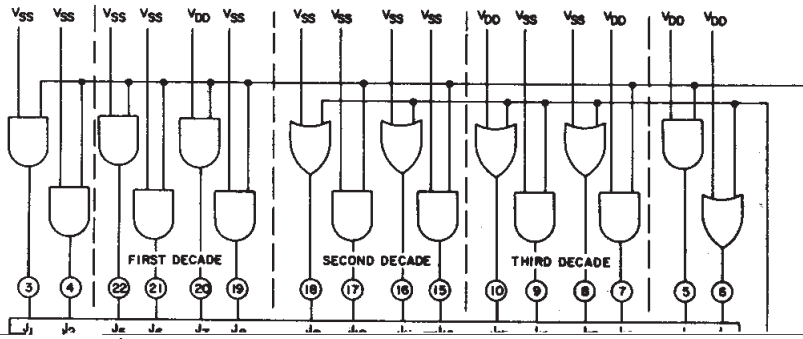
For changing from any mode other than mode 5 (with power on), apply positive pulse to C_{in}. This circuit automatically selects master preset mode ($K_b = 0$, $K_c = 0$) before going into the select conditions for mode 5 ($K_a = 1$, $K_b = 0$, $K = 1$). The selection of C_1 and C_2 is critical. C_1 is determined by the VDD voltage--the lower VDD's need larger C_1's. C_2 must be 0.1 μF or larger.

Fig.21 - CD4059A mode 5 power on master preset circuit.
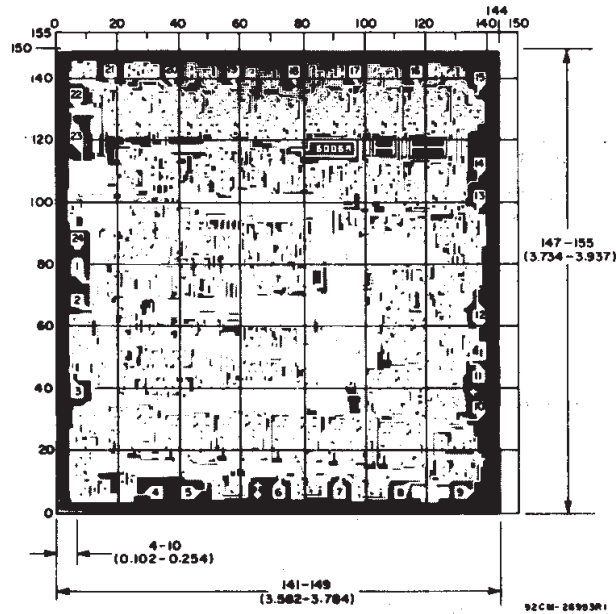
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

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