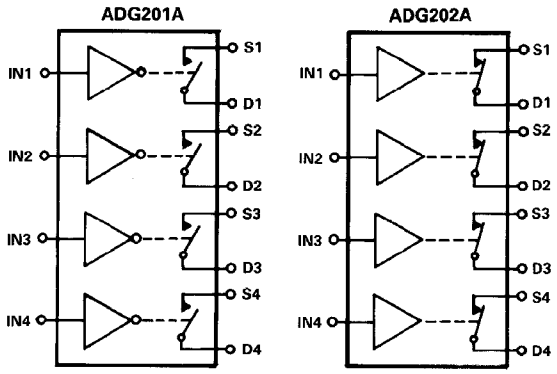
# LC²MOS Quad SPST Switches

# ADG201A/ADG202A

**FEATURES**
- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low $R_{ON}$ (60Ω)
- Low Leakage (0.5nA)
- Break Before Make Switching
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (33mW)
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Superior Second Source:
  - ADG201A Replaces DG201A, HI-201
  - ADG202A Replaces DG202

**FUNCTIONAL BLOCK DIAGRAMS**




SWITCHES SHOWN FOR A LOGIC "1" INPUT

## GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also

## PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.

3. Low Leakage:

# ADG201A/ADG202A—SPECIFICATIONS ($V_{DD}$ = +15V, $V_{SS}$ = −15V, unless otherwise specified)

| Parameter | K Version 25°C | K Version −40°C to +85°C | B Version 25°C | B Version −40°C to +85°C | T Version 25°C | T Version −55°C to +125°C | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | | | |
| Analog Signal Range | ±15 | ±15 | ±15 | ±15 | ±15 | ±15 | Volts | |
| $R_{ON}$ | 60 | | 60 | | 60 | | Ω typ | $-10V \leq V_S \leq +10V$ |
| | 90 | 145 | 90 | 145 | 90 | 145 | Ω max | $I_{DS}$ = 1.0mA |
| | | | | | | | | Test Circuit 1 |
| $R_{ON}$ vs. $V_D$ ($V_S$) | 20 | | 20 | | 20 | | % typ | |
| $R_{ON}$ Drift | 0.5 | | 0.5 | | 0.5 | | %/°C typ | |
| $R_{ON}$ Match | 5 | | 5 | | 5 | | % typ | $V_S$ = 0V, $I_{DS}$ = 1mA |
| $I_S$ (OFF) | 0.5 | | 0.5 | | 0.5 | | nA typ | $V_D = \pm 14V$; $V_S \mp 14V$; Test Circuit 2 |
| OFF Input Leakage | 2 | 100 | 2 | 100 | 1 | 100 | nA max | |
| $I_D$ (OFF) | 0.5 | | 0.5 | | 0.5 | | nA typ | $V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2 |
| OFF Output Leakage | 2 | 100 | 2 | 100 | 1 | 100 | nA max | |
| $I_D$ (ON) | 0.5 | | 0.5 | | 0.5 | | nA typ | $V_D = \pm 14V$; Test Circuit 3 |
| ON Channel Leakage | 2 | 200 | 2 | 200 | 1 | 200 | nA max | |
| DIGITAL CONTROL | | | | | | | | |
| $V_{INH}$, Input High Voltage | | 2.4 | | 2.4 | | 2.4 | V min | |
| $V_{INL}$, Input Low Voltage | | 0.8 | | 0.8 | | 0.8 | V max | |
| $I_{INL}$ or $I_{INH}$ | | 1 | | 1 | | 1 | μA max | |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| $t_{OPEN}$ | 30 | | 30 | | 30 | | ns typ | |
| $t_{ON}$[1] | 300 | | 300 | | 300 | | ns max | Test Circuit 4 |
| $t_{OFF}$[1] | 250 | | 250 | | 250 | | ns max | Test Circuit 4 |
| OFF Isolation | 80 | | 80 | | 80 | | dB typ | $V_S$ = 10V(p-p); f = 100kHz |
| | | | | | | | | $R_L$ = 75Ω; Test Circuit 6 |
| Channel-to-Channel Crosstalk | 80 | | 80 | | 80 | | dB typ | Test Circuit 7 |
| $C_S$ (OFF) | 5 | | 5 | | 5 | | pF typ | |
| $C_D$ (OFF) | 5 | | 5 | | 5 | | pF typ | |
| $C_D$, $C_S$ (ON) | 16 | | 16 | | 16 | | pF typ | |
| $C_{IN}$ Digital Input Capacitance | 5 | | 5 | | 5 | | pF typ | |
| $Q_{INJ}$ Charge Injection | 20 | | 20 | | 20 | | pC typ | $R_S$ = 0Ω; $C_L$ = 1000pF; $V_S$ = 0V |
| | | | | | | | | Test Circuit 5 |
| POWER SUPPLY | | | | | | | | |
| $I_{DD}$ | 0.6 | | 0.6 | | 0.6 | | mA typ | Digital Inputs = $V_{INL}$ or $V_{INH}$ |
| $I_{DD}$ | | 2 | | 2 | | 2 | mA max | |
| $I_{SS}$ | 0.1 | | 0.1 | | 0.1 | | mA typ | |
| $I_{SS}$ | | 0.2 | | 0.2 | | 0.2 | mA max | |
| Power Dissipation | | 33 | | 33 | | 33 | mW max | |

NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS*

($T_A$ = +25°C unless otherwise stated)

$V_{DD}$ to $V_{SS}$ . . . . . 44V
$V_{DD}$ to GND . . . . . 25V
$V_{SS}$ to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . $V_{SS}$ −0.3V to $V_{DD}$ +0.3V
Continuous Current, S or D . . . . . 30mA
Pulsed Current S or D

Power Dissipation (Any Package)
Up to +75°C . . . . . 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

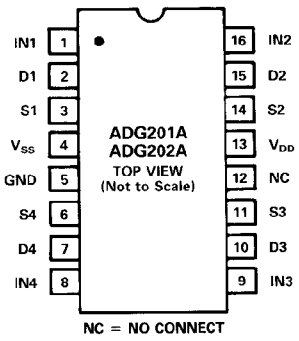

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Option[2] |
|---|---|---|
| ADG201AKN | −40°C to +85°C | N-16 |
| ADG201AKR | −40°C to +85°C | R-16A |
| ADG201AKP | −40°C to +85°C | P-20A |
| ADG201ABQ | −40°C to +85°C | Q-16 |
| ADG201ATQ | −55°C to +125°C | Q-16 |
| ADG201ATE | −55°C to +125°C | E-20A |
| ADG202AKN | −40°C to +85°C | N-16 |
| ADG202AKR | −40°C to +85°C | R-16A |
| ADG202AKP | −40°C to +85°C | P-20A |
| ADG202ABQ | −40°C to +85°C | Q-16 |
| ADG202ATQ | −55°C to +125°C | Q-16 |
| ADG202ATE | −55°C to +125°C | E-20A |

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

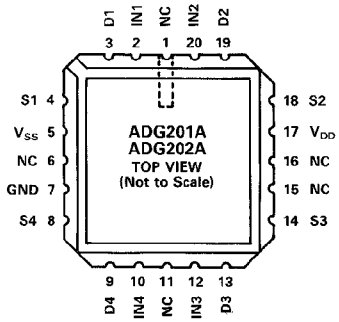
## PIN CONFIGURATIONS

### DIP, SOIC



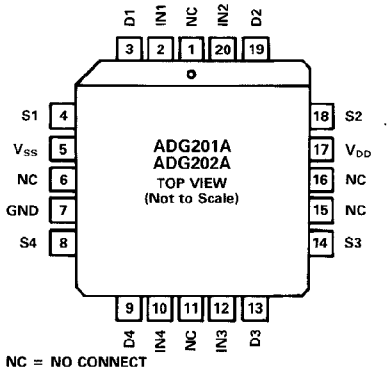

NC = NO CONNECT

### LCCC



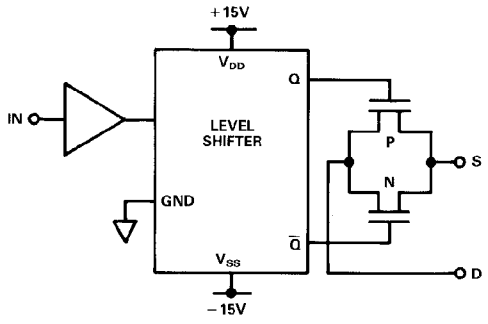

NC = NO CONNECT

### PLCC




NC = NO CONNECT

## ADG201A/ADG202A FUNCTIONAL DIAGRAM



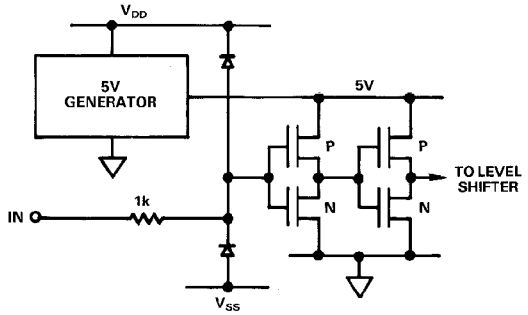
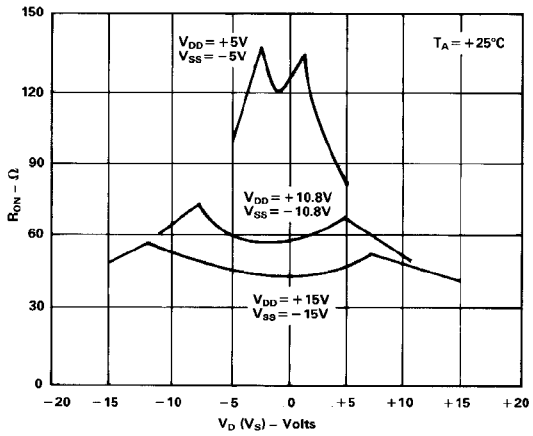



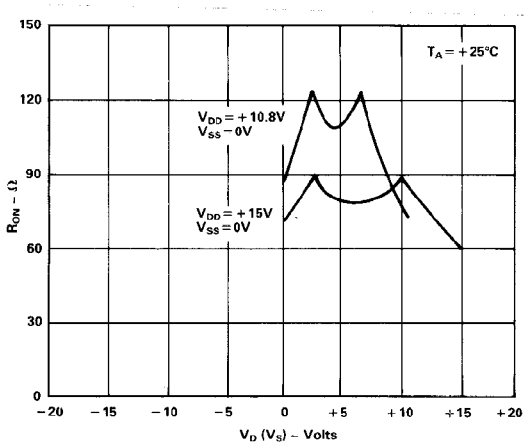

*Figure 1. Typical Digital Input Cell*

# ADG201A/ADG202A—Typical Performance Characteristics

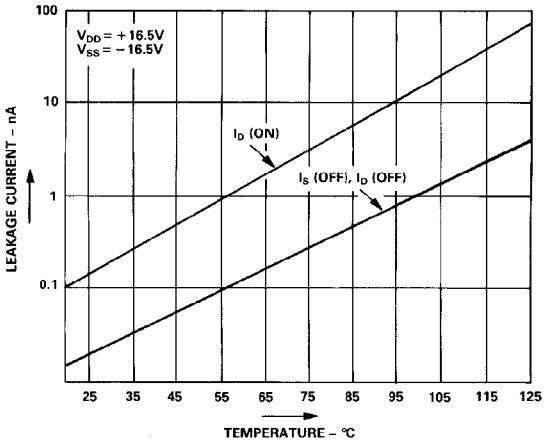
**The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.**



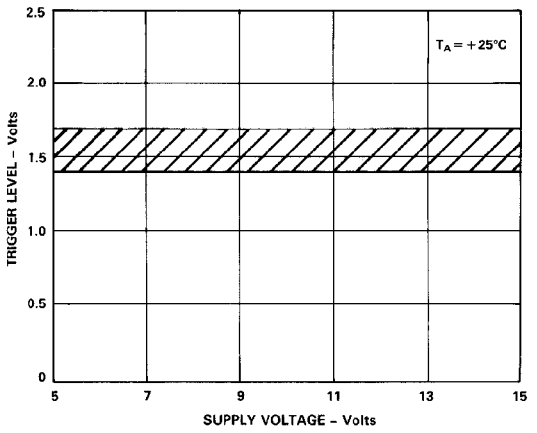

*$R_{ON}$ as a Function of $V_D$ ($V_S$): Dual Supply Voltage*



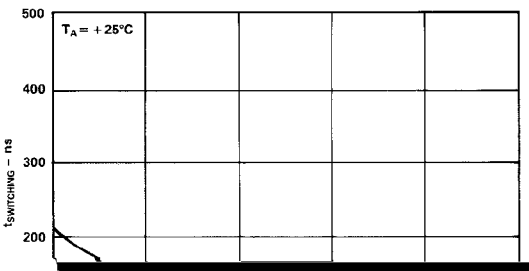

*$R_{ON}$ as a Function of $V_D$ ($V_S$): Single Supply Voltage*

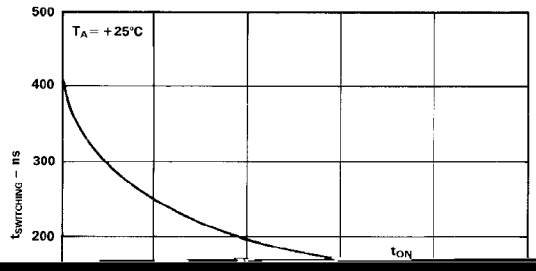


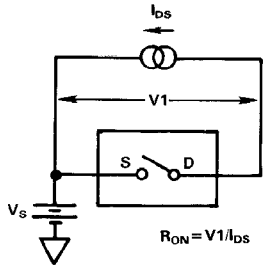

*Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)*



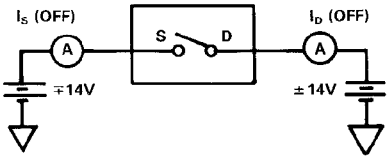

*Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage*



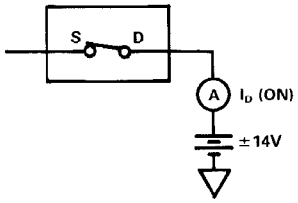





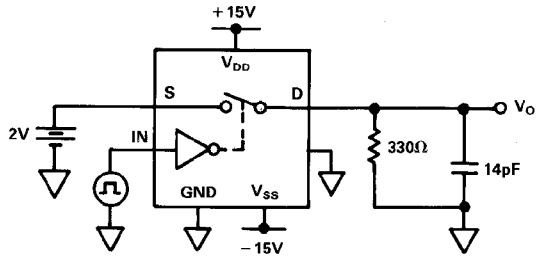

Test Circuit 1

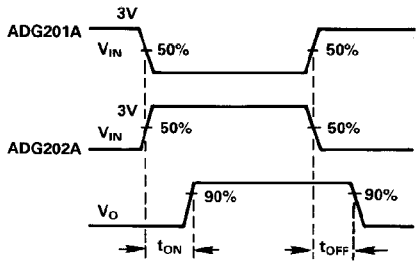



Test Circuit 2

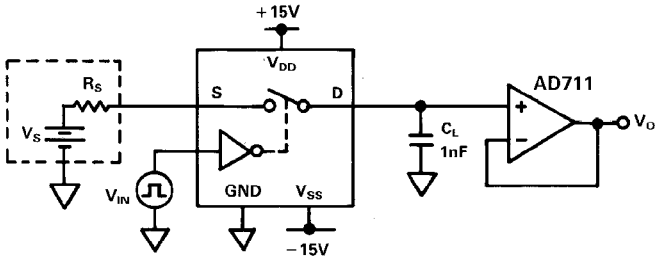


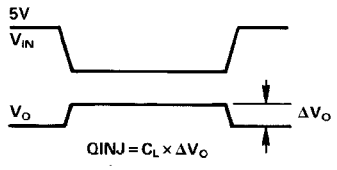

Test Circuit 3



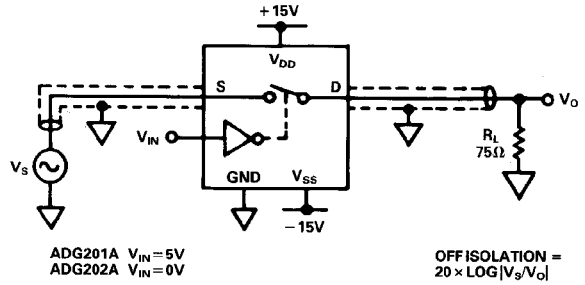




Test Circuit 4

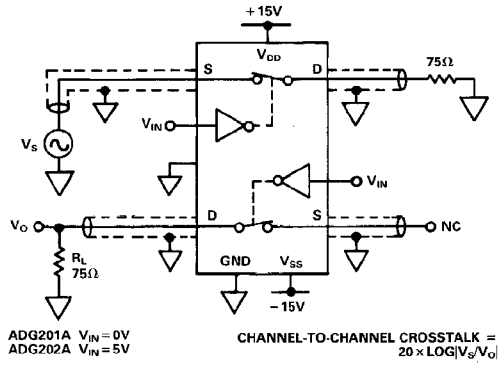



Test Circuit 5. Charge Injection




Test Circuit 6. Off Isolation




Test Circuit 7. Channel-to-Channel Crosstalk

## TERMINOLOGY

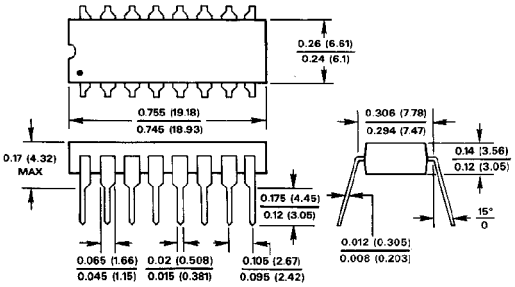
| | |
|---|---|
| $R_{ON}$ | Ohmic resistance between terminals OUT and S |
| $R_{ON}$ Match | Difference between the $R_{ON}$ of any two channels |
| $I_S$ (OFF) | Source terminal leakage current when the switch is off |
| $I_D$ (OFF) | Drain terminal leakage current when the switch is off |
| $I_D$ (ON) | Leakage current that flows from the closed switch into the body |
| $V_D$ ($V_S$) | Analog voltage on terminal D, S |
| $C_S$ (OFF) | Switch input capacitance "OFF" condition |
| $C_D$ (OFF) | Switch output capacitance "OFF" condition |
| $C_{IN}$ | Digital input capacitance |
| $C_D$, $C_S$ (ON) | Input or output capacitance when the switch is on |
| $t_{ON}$ | Delay time between the 50% and 90% points of the digital input and switch "ON" condition |
| $t_{OFF}$ | Delay time between the 50% and 90% points of the digital input and switch "OFF" condition |
| $t_{OPEN}$ | "OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another |
| $V_{INL}$ | Maximum Input Voltage for a Logic Low |
| $V_{INH}$ | Minimum Input Voltage for a Logic High |
| $I_{INL}$ ($I_{INH}$) | Input current of the digital input |
| $V_{DD}$ | Most positive voltage supply |
| $V_{SS}$ | Most negative voltage supply |
| $I_{DD}$ | Positive supply current |
| $I_{SS}$ | Negative supply current |

## MECHANICAL INFORMATION

### OUTLINE DIMENSIONS

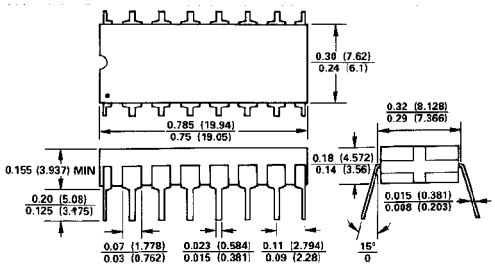
Dimensions shown in inches and (mm).

**16-Pin Plastic (N-16)**

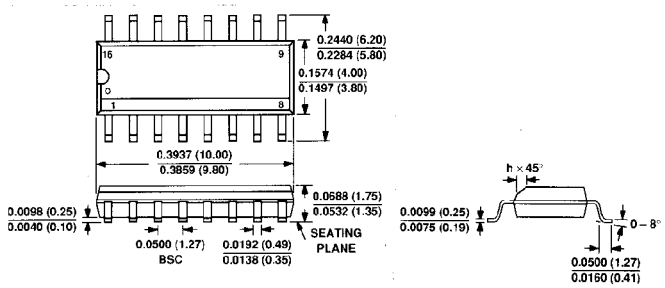



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

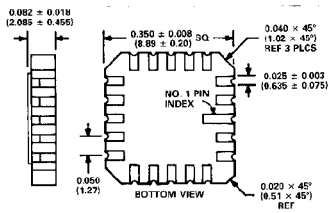
**16-Pin Cerdip (Q-16)**




**SOIC Package (R-16A)**




**20-Terminal Leadless Ceramic Chip Carrier (E-20A)**




**20-Terminal Plastic Leaded Chip Carrier (P-20A)**