National Semiconductor

MM5309, MM5311, MM5312, MM5313, MM5314, MM5315 Digital Clocks

General Description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion implanted, depletion mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (4 or 6-digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11V to 19V and do not require a regulated supply. These clocks are packaged in dual-in-line packages.

Features

- 50 or 60 Hz operation
- 12 or 24-hour display format
- Leading-zero blanking (12-hour format)
- 7-segment outputs
- Single power supply
- Fast and slow set controls
- Internal multiplex oscillator
- For features of individual clocks, see Table I

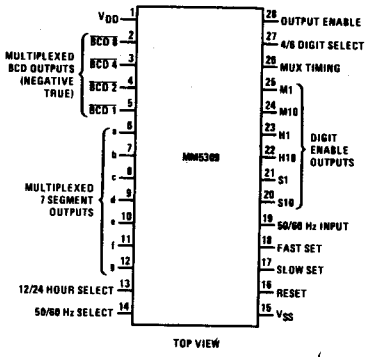
Applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Interval Timers

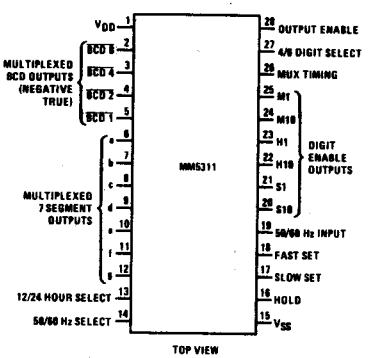
TABLE I

FEATURES	MM5309	MM5311	MM5312	MM5313	MM5314	MM5315
$\overline{BCD}$ Outputs	X	X	X	X		X
4/6-Digit Display Mode	X	X		X	X	X
Hold Count Control		X		X	X	X
1 Hz Output			X	X		
Output Enable Control	X	X			X	
Reset	X					X

Connection Diagrams (Dual-In-Line Packages)



Order Number MM5309N
See Package 23



Order Number MM5311N
See Package 23

Absolute Maximum Ratings

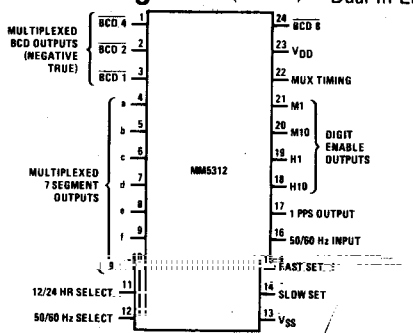
Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} −20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

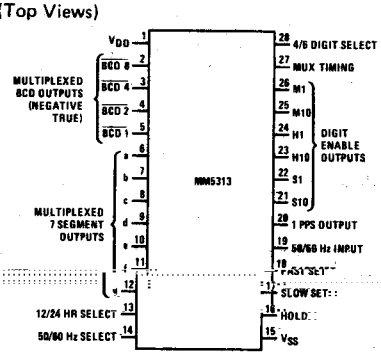
T_A within operating range, V_{SS} = 11V to 19V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11		19	V
Power Supply Current	V_{SS} = 14V, (No Output Loads)			10	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
Multiplex Frequency	Determined by External R & C	0.100	1.0	60	kHz
All Logic Inputs	Driven by External Timebase	dc		60	kHz
Logical High Level	Internal Depletion Device to V_{SS}	V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2 kΩ to V_{DD}	2.0		20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100 Ω to V_{SS}	5.0		25	mA sink

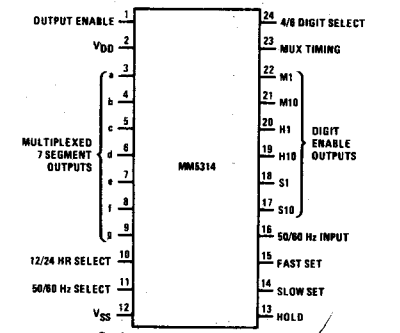
Connection Diagrams (Cont'd) Dual-In-Line Packages (Top Views)



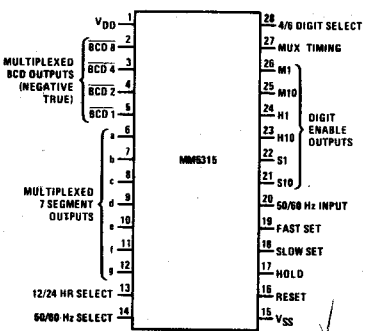
Order Number MM5312N
See Package 22



Order Number MM5313N
See Package 23



Order Number MM5314N
See Package 22



Order Number MM5315N
See Package 23

Functional Description

A block diagram of the MM5309 digital clock is shown in *Figure 1*. MM5311, MM5312, MM5313, MM5314 and MM5315 clocks are bonding options of MM5309 clock. Table I shows the pin-outs for these clocks.

50 or 60 Hz Input: This input is applied to a Schmitt Trigger shaping circuit which provides approximately 5V of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 10* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 Hz timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal depletion device is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in *Figure 1*, the prescale counter provides both 1 Hz and 10 Hz signals, which can be brought out as bonding options.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal depletion devices provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain *(Figure 1)* are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷50 or ÷60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24-Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal depletion device) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a 6-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6-digit select input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{BCD}$ and 7-segment. The sequential output order is from digit 6 (unit seconds) through digit 1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in *Figure 2*. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in *Figure 4a*) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt Trigger in *Figure 2*. *Figure 3* provides guidelines for selecting the external components relative to desired multiplex frequency.

Figure 4 also illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as 50 or 60 Hz input.

Reset: Applying V_{DD} to this input resets the counters to 0:00:00.00 in 12-hour format and 00:00:00.00 in 24-hour formats leaving the input unconnected (internal depletion pull-up) selects normal operation. Proper reset will be ensured when V_{DD} to V_{SS} slew rate is no faster than one volt per microsecond. This can be accomplished with a capacitor from the reset input to V_{SS}.

4 or 6-Digit Select Input: Like the other control inputs, this input is provided with an internal depletion pull-up device. With no input connection the clock outputs data for a 4-digit display. Applying V_{DD} to this input provides a 6-digit display.

Output Enable Input: With this pin unconnected the $\overline{BCD}$ and 7-segment outputs are enabled (via an internal depletion pull-up). Switching V_{DD} to this input inhibits these outputs. (Not applicable to MM5312, MM5313, and MM5315 clocks.)

Output Circuits: *Figure 5a* illustrates the circuit used for the $\overline{BCD}$ and 7-segment outputs. *Figure 5b* shows the digit enable output circuit. *Figure 6* illustrates interfacing these outputs to standard and low power TTL. *Figures 7 and 8* illustrate methods of interfacing these outputs to common anode and common cathode LED displays, respectively. A method of interfacing these clocks to gas discharge display tubes is shown in *Figure 9*. When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. *Figure 9* also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

Functional Description (Cont'd)

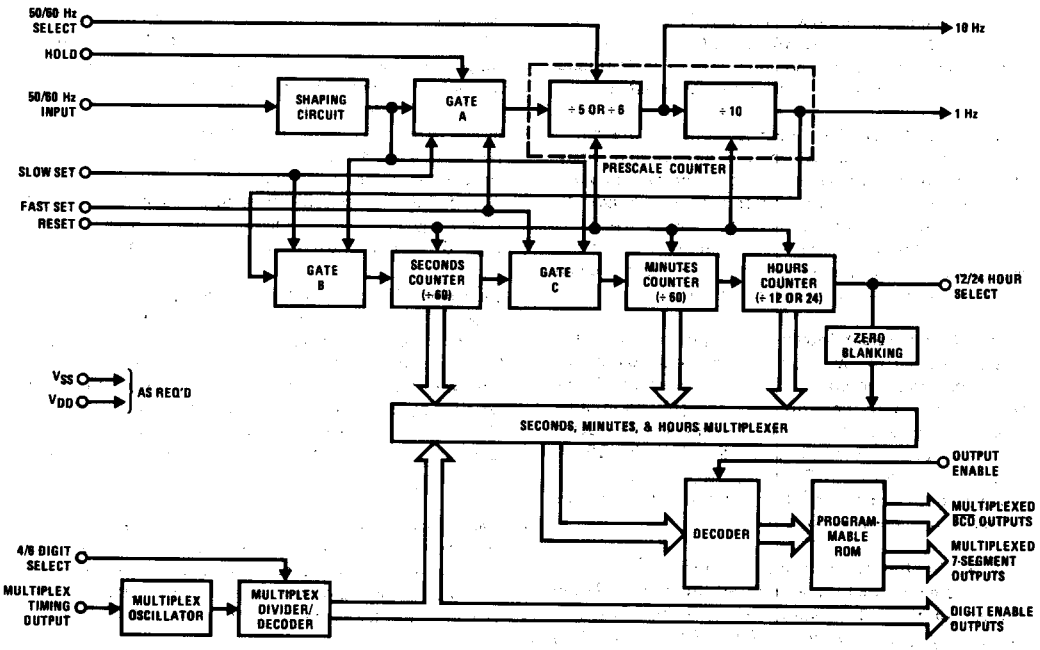


FIGURE 1. MM5309 Digital Clock Block Diagram

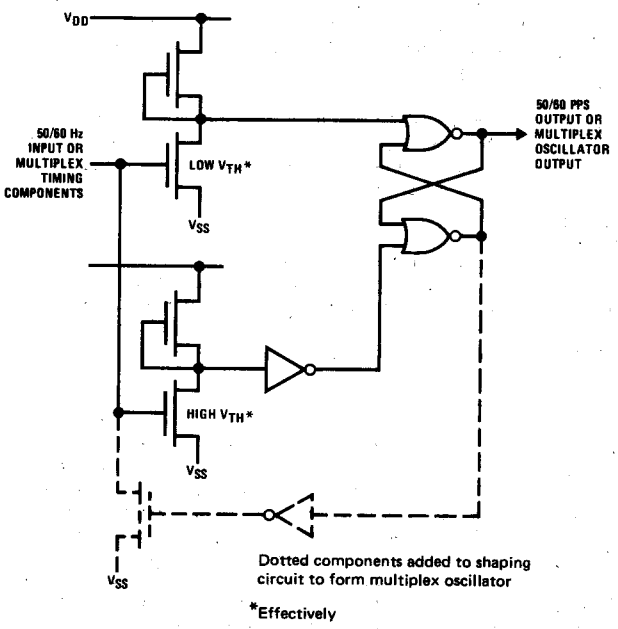


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

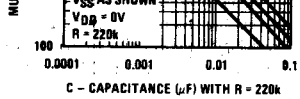


FIGURE 3. Multiplex Timing Component Selection Guide

Functional Description (Cont'd)

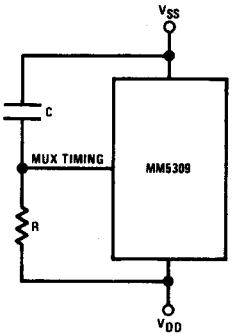


FIGURE 4a. Relaxation Oscillator

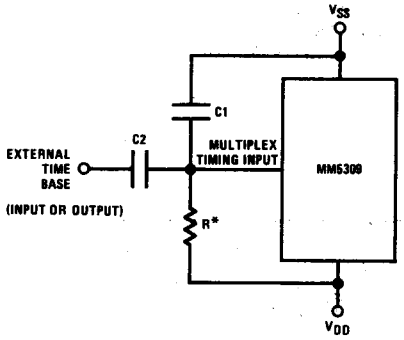


FIGURE 4b. External Time Base

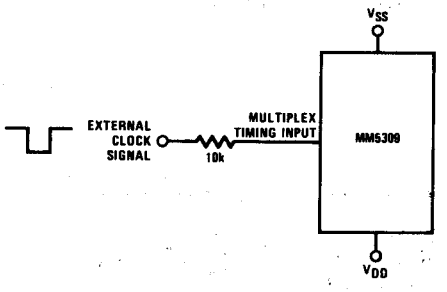


FIGURE 4c. External Clock

Note. Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.
* R=100k.

FIGURE 4. Synchronizing or Triggering Multiplex Oscillators

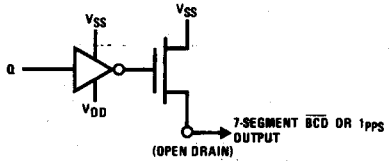


FIGURE 5a

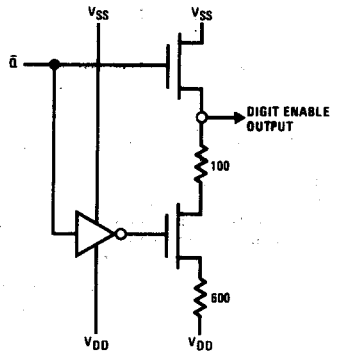
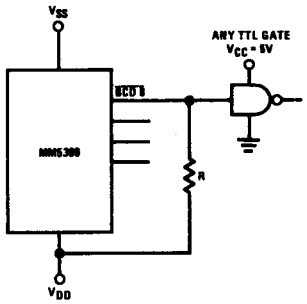


FIGURE 5b

FIGURE 5. Output Circuits

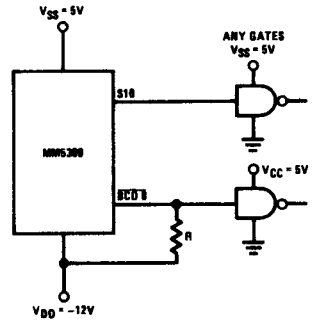
Functional Description (Cont'd)

MOS to Low Power TTL Interface



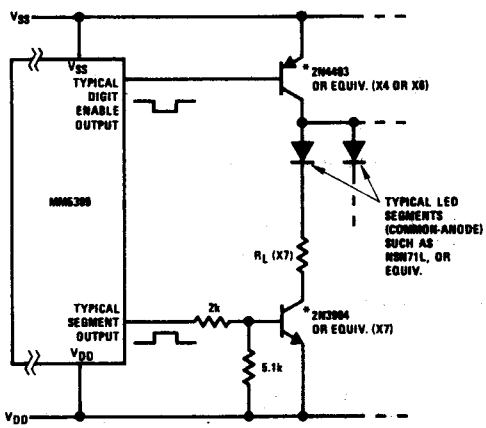
For V_{SS} = 5, V_{DD} = 12, R = 10k
For V_{SS} = 10 to 17V, V_{DD} = Gnd, R = 3k

MOS to TTL Interface



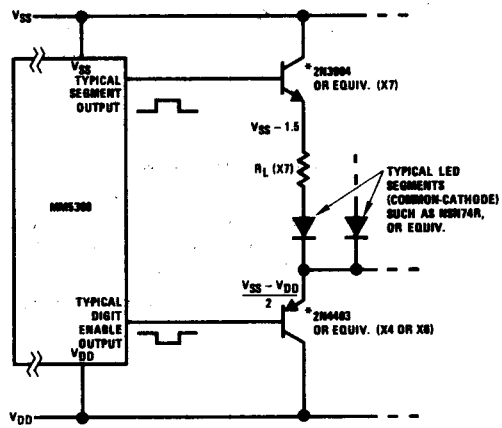
For V_{SS} = 5, V_{DD} = −12, R = 7.5k
Note. Digit select will drive TTL directly when 5, −12 supplies are used.

FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} - V_{DD} - V_F - 0.6V}{N(I_F)}$$

Where R_L as in kΩ
And V_F = forward drop of LED
0.6V ≈ voltage drop of transistors
N = number of digits in display
I_F = required average LED current



$$R_L = \frac{V_{SS}\ V_{DD})/2\ V_F\ 1.5V}{N(I_F)}$$

Where R_L is in kΩ
And V_F = forward drop of LED
0.9V = voltage drop of transistors
N = number of digits in display
I_F = required average LED current

*Transistors may be replaced by DM75491, DM75492, DM8861, DM8863 or equivalent segment/digit drivers.

FIGURE 7. Interfacing Common Anode LED Displays

FIGURE 8. Interfacing Common Cathode LED Displays

Functional Description (Cont'd)

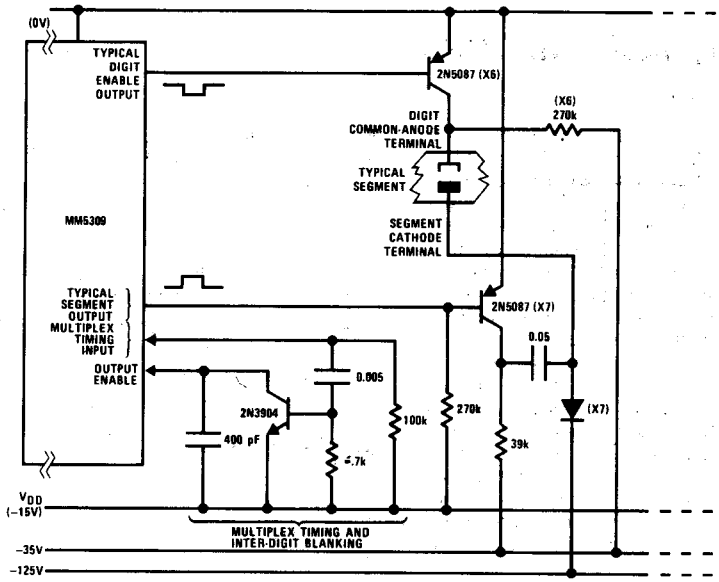


FIGURE 9. Interface Panaplex II* Neon Display Tube

*TM of Burroughs Corp.

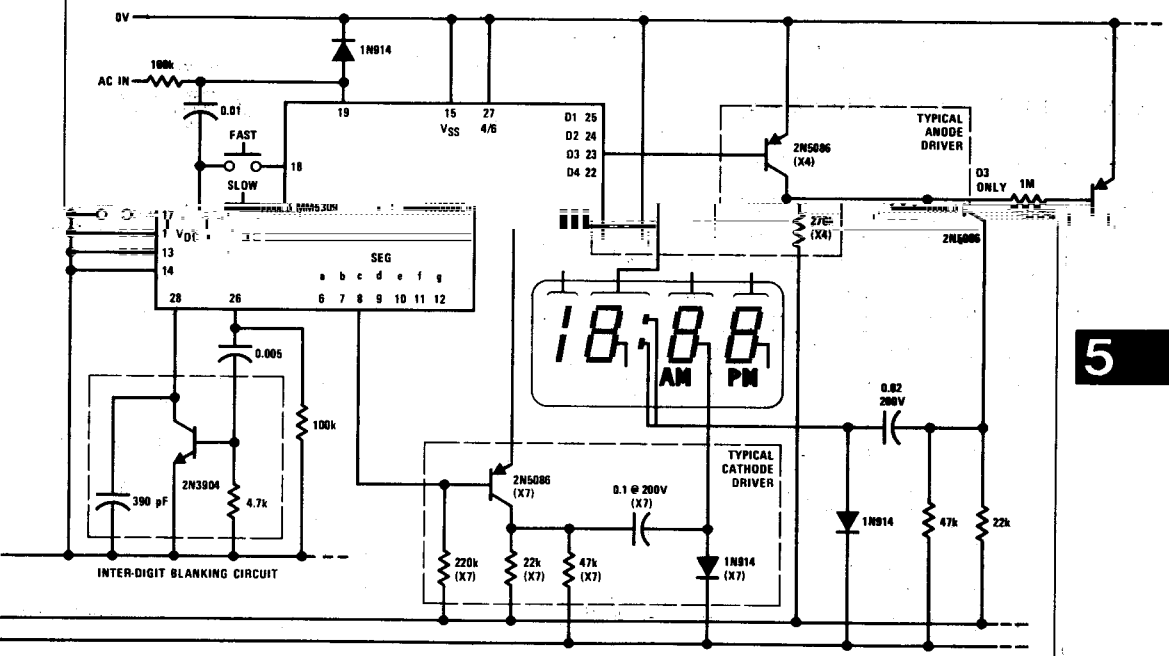


FIGURE 10. MM5309 Driving Gas Discharge Display, Typical Applications

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