6N140A,* HCPL-675X, 83024, HCPL-570X, HCPL-177K, 5962-89810, HCPL-573X, HCPL-673X, 5962-89785, 5962-98002

Hermetically Sealed, Low I_F, Wide V_{CC}, High Gain Optocouplers

Data Sheet

*See matrix for available extensions.

Description

These units are single, dual, and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DLA Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional photo transistor optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers. Compatibility with high voltage CMOS logic systems is assured by specifying I_{CCH} and I_{OH} at 18 Volts.

Features

- Dual marked with device part number and DLA drawing number
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Five hermetically sealed package configurations
- Performance guaranteed over full military temperature range: -55°C to +125°C
- Low input current requirement: 0.5 mA
- High current transfer ratio: 1500% typical @ I_F = 0.5 mA
- Low output saturation voltage: 0.11 V typical
- 1500 Vdc withstand test voltage
- High radiation immunity
- 6N138/9, HCPL-2730/31 function compatibility
- Reliability data

Applications

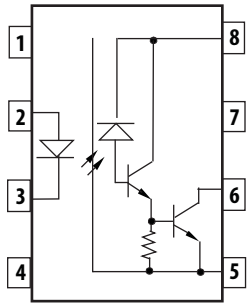
- Military and aerospace
- High reliability systems
- Telephone ring detection
- Microprocessor system interface
- Transportation, medical, and life critical systems
- Isolated input line receiver
- EIA RS-232-C line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Current loop receiver
- System test equipment isolation
- Process control input/output isolation

The connection of a 0.1 μF bypass capacitor between V_{CC} and GND is recommended.

***CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Functional Diagram

Multiple Channel Devices Available



Truth Table

(Positive Logic)

Input	Output
On (H)	L
O□ (L)	H

Upon special request, the following device selections can be made: CTR minimum of up to 600% at 0.5 mA, and lower output leakage current levels to 100 μA.

Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), 16 pin DIP □at pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical speci□cations, and performance characteristics shown in the □gures are similar for all parts except as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities justify the use of a common data base for die related reliability and certain limited radiation test results.

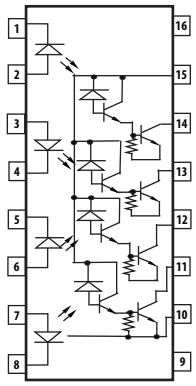
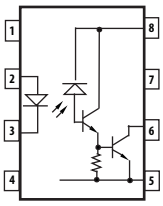
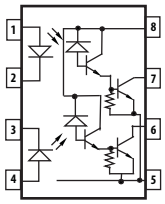
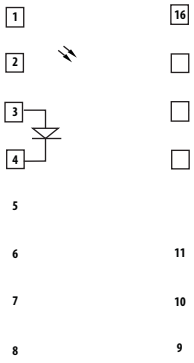
Selection Guide-Package Styles and Lead Configuration Options

Package	16 pin DIP	8 pin DIP	8 pin DIP	16 pin Flat Pack	20 Pad LCCC
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	4	1	2	4	2
Common Channel Wiring	V_{CC}, GND	None	V_{CC}, GND	V_{CC}, GND	None
Avago Part # & Options					
Commercial	6N140A[1]	HCPL-5700	HCPL-5730	HCPL-6750	HCPL-6730
MIL-PRF-38534 Class H	6N140A/883B	HCPL-5701	HCPL-5731	HCPL-6751	HCPL-6731
MIL-PRF-38534 Class K	HCPL-177K	HCPL-570K	HCPL-573K	HCPL-675K	HCPL-673K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Solder Pads*
Solder Dipped*	Option #200	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100	Option #100		
Gull Wing/Soldered*	Option #300	Option #300	Option #300		
Crew Cut/Gold Plate	Option #600	Option #600	Option #600		
Class H SMD Part #					
Prescript for all below	*None*	*5962-*	*5962-*	*None*	*5962-*
Gold Plate	8302401EC	8981001PC	8978501PC	8302401FC	
Solder Dipped*	8302401EA	8981001PA	8978501PA		89785022A
Butt Cut/Gold Plate	8302401YC	8981001YC	8978501YC		
Butt Cut/Soldered*	8302401YA	8981001YA	8978501YA		
Gull Wing/Soldered*	8302401XA	8981001XA	8978501ZA		
Crew Cut/Gold Plate	8302401ZC	Available	Available		
Crew Cut/Soldered*	8302401ZA	Available	Available		
Class K SMD Part #					
Prescript for all below	*5962-*	*5962-*	*5962-*	*5962-*	*5962-*
Gold Plate	9800201KEC	8981002KPC	8978503KPC	9800201KFC	
Solder Dipped*	9800201KEA	8981002KPA	8978503KPA		8978504K2A
Butt Cut/Gold Plate	9800201KYC	8981002KYC	8978503KYC		
Butt Cut/Soldered*	9800201KYA	8981002KYA	8978503KYA		
Gull Wing/Soldered*	9800201KXA	8981002KXA	8978503KZA		
Crew Cut/Gold Plate	9800201KZC	Available	Available		
Crew Cut/Soldered*	9800201KZA	Available	Available		

*Solder contains lead.

Note:
1. JEDEC registered part.

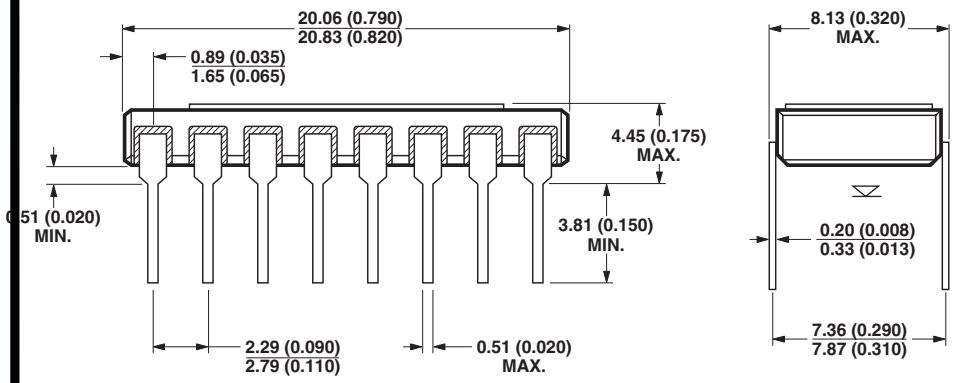
Functional Diagrams

16 pin DIP	8 pin DIP	8 pin DIP	16 pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
4 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

Note: All DIP and flat pack devices have common V_{CC} and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

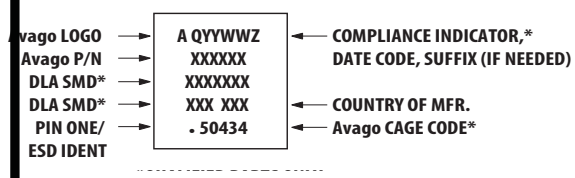
Outline Drawings

16 Pin DIP Through Hole, 4 Channels

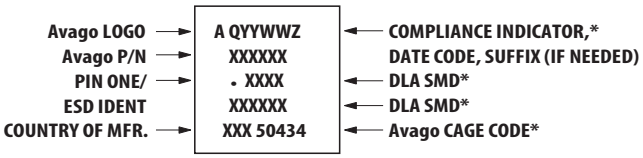


Note: Dimensions in Millimeters (Inches)

Leaded Device Marking

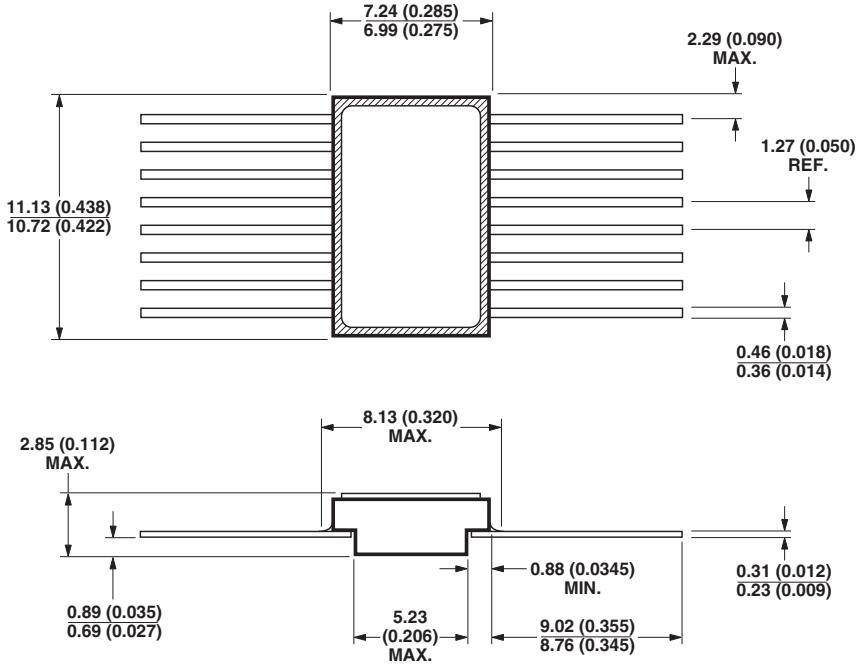


Leadless Device Marking



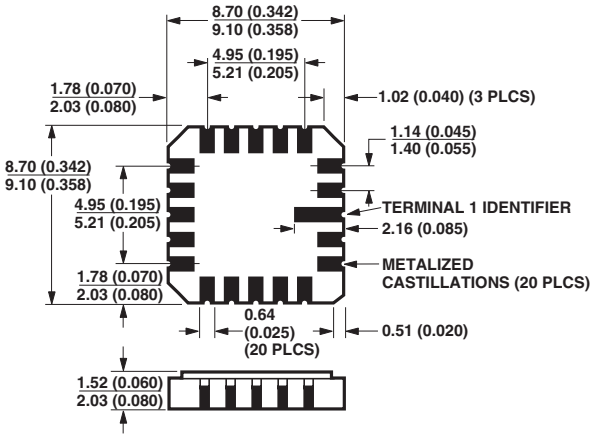
Outline Drawings (continued)

16 Pin Flat Pack, 4 Channels



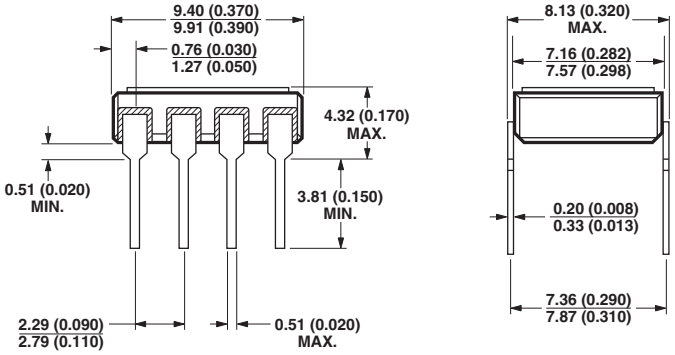
Note: Dimensions in Millimeters (Inches)

20 Terminal LCCC Surface Mount, 2 Channels



Note: Dimensions in Millimeters (Inches).
Solder Thickness 0.127 (0.005) Max.

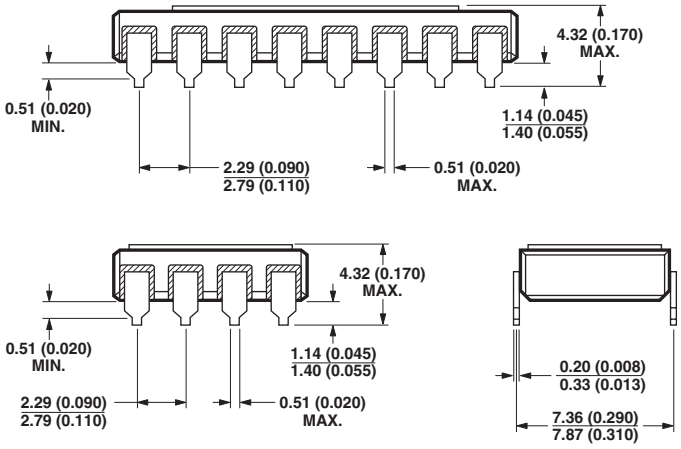
8 Pin DIP Through Hole, 1 and 2 Channel



Note: Dimensions in Millimeters (Inches).

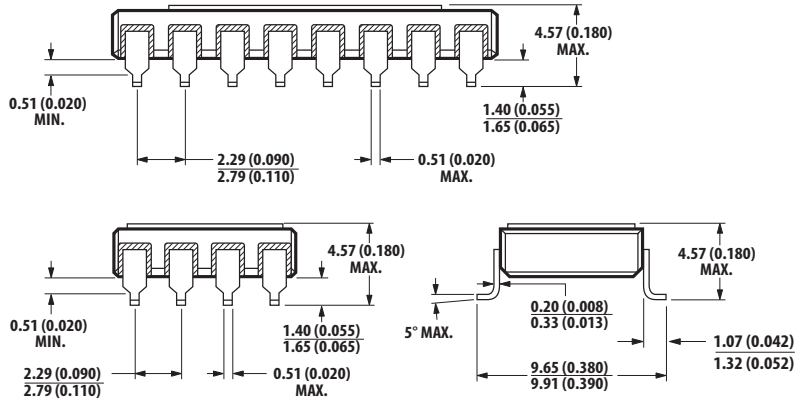
Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).



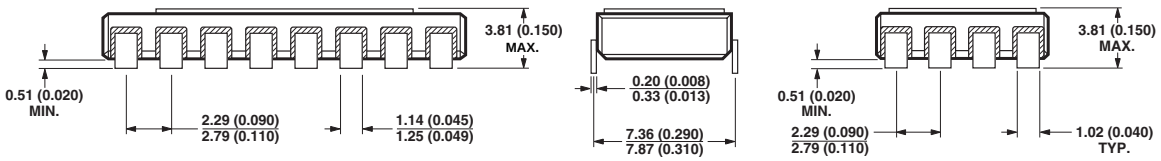
Note: Dimensions in Millimeters (Inches).

200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DLA Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.



Note: Dimensions in Millimeters (Inches).

600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DLA part types.



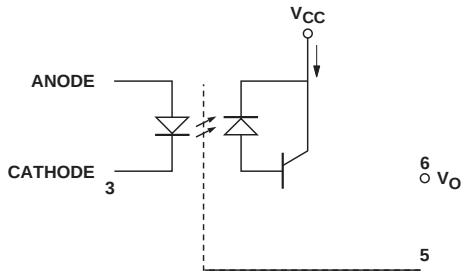
Note: Dimensions in Millimeters (Inches).

Solder contains lead.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Case Temperature	T_C		+170	°C	
Junction Temperature	T_J		+175	°C	
Lead Solder Temperature			260 for 10 sec	°C	
Output Current (each channel)	I_O		40	mA	
Output Voltage (each channel)	V_O	-0.5	20	V	1
Supply Voltage	V_{CC}	-0.5	20	V	1
Output Power Dissipation (each channel)			50	mW	2
Peak Input Current (each channel, <1 ms duration)			20	mA	
Average Input Current (each channel)	I_F		10	mA	3
Reverse Input Voltage (each channel)	V_R		5	V	
Package Power Dissipation (each channel)	P_D		200	mW	

8 Pin Ceramic DIP Single Channel Schematic



ESD Classification

(MIL-STD-883, Method 3015)

HCPL-5700/01/0K and 6730/31/3K	(▲▲), Class 2
6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K and HCPL-5730/31/3K	(Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F(OFF)}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F(ON)}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V
Output Voltage	V_O	2.0	18	V

Electrical Characteristics, T_A = -55°C to +125°C, unless otherwise specified

Parameter		Symbol	Test Conditions	Group A[13] Subgroup	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Current Transfer Ratio		CTR*	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		300	1000				
			I_F =5 mA, V_O = 0.4 V, V_{CC} = 4.5 V		200	500				
Logic Low Output Voltage		V_{OL}	I_F = 0.5 mA, I_{OL} = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.11	0.4	V	2	4
			I_F = 1.6 mA, I_{OL} = 4.8 mA, V_{CC} = 4.5 V			0.13	0.4			4, 16
			I_F =5 mA, I_{OL} = 10 mA, V_{CC} = 4.5 V			0.16	0.4			4
Logic High Output Current		I_{OH}*	I_F =2 µA, V_O = 18 V, V_{CC} = 18 V	1, 2, 3		0.001	250	µA		4
		I_{OHX}					250	µA		4, 6
Logic Low Supply Current	Single Channel and LCCC	I_{CCL}*	I_F =1.6 mA, V_{CC} = 18 V	1, 2, 3		1.0	2	mA		15
	Dual Channel		I_{F1} =I_{F2} = 1.6 mA, V_{CC} = 18 V			1.0	4		4	
	Quad Channel		I_{F1} = I_{F2} =I_{F3} =I_{F4} =1.6 mA, V_{CC} = 18 V			1.7	4			
Logic High Supply Current	Single Channel and LCCC	I_{CCH}*	I_F =0 mA, VCC = 18 V	1, 2, 3		0.001	20	µA		15
	Dual Channel		I_{F1} =I_{F2} = 0 mA, V_{CC} = 18 V				40			
	Quad Channel		I_{F1} = I_{F2} =I_{F3} =I_{F4} =0 mA, V_{CC} = 18 V				40			
Input Forward Voltage	Single and Dual Channel	V_F*	I_F = 1.6 mA	1	1.0	1.4	1.7	V	1	4
				2			1.7			
				3			1.8			
	LCCC			1, 2, 3	1.0	1.4	1.8			
	Quad Channel			1, 2		1.4	1.7			
				3			1.8			
Input Reverse Breakdown Voltage		B_{VR}*	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current		I_{I-O}*	≤65% Relative Humidity T_A =25°C, t = 5 s, V_{I-O} = 1500 VDC	1			1.0	µA		7, 12
Capacitance Between Input-Output		C_{I-O}	f= 1 MHz, T_A =25°C	4			4	pF		4, 8 14, 17

* For JEDEC registered parts.

** All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus total supply power for the single channel device. For the dual channel device, output power is collector output power plus one half the total supply power. For the quad channel device, output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is de□ned as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. $I_F = 2$ µA for channel under test. For all other channels, $I_F = 10$ mA.
7. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
8. Measured between each input pair shorted together and all output connections for that channel shorted together.
9. Measured between adjacent input pairs shorted together for each multi-channel device.
10. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8$ V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0$ V).
11. In applications where dV/dt may exceed 50,000 V/µs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is:

    $$R_{CC} = \frac{1\ (V)}{0.15\ I_F\ (mA)}\ k\Omega$$

    for single channel;

    $$R_{CC} = \frac{1\ (V)}{0.3\ I_F\ (mA)}\ k\Omega$$

    for dual channel;

    $$R_{CC} = \frac{1\ (V)}{0.6\ I_F\ (mA)}\ k\Omega$$

    for quad channel.
12. This is a momentary withstand test, not an operating condition.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25,125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
14. Parameters tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits speci□ed for all lots not speci□cally tested.
15. The HCPL-6730, HCPL-6731, and HCPL-673K dual channel parts function as two independent single channel units. Use the single channel parameter limits.
16. Not required for 6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K, 8302401, and 5962-9800201 types.
17. Required for 6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K, 8302401, and 5962-9800201 types.

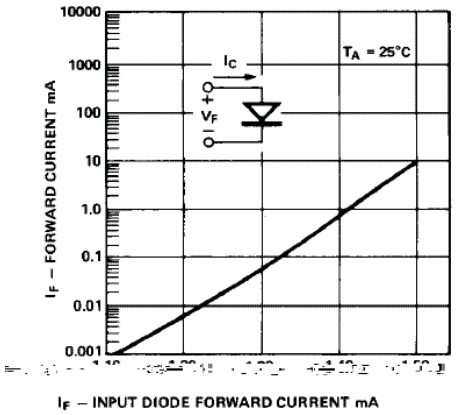


Figure 1. Input Diode Forward Current vs. Forward Voltage.

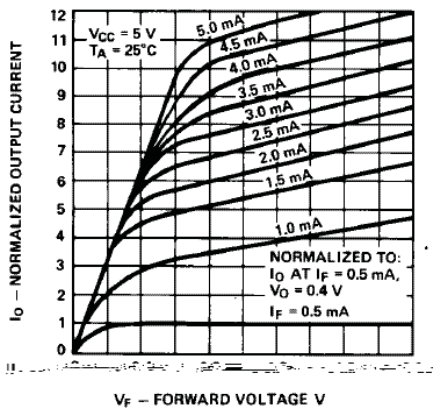


Figure 2. Normalized DC Transfer Characteristics.

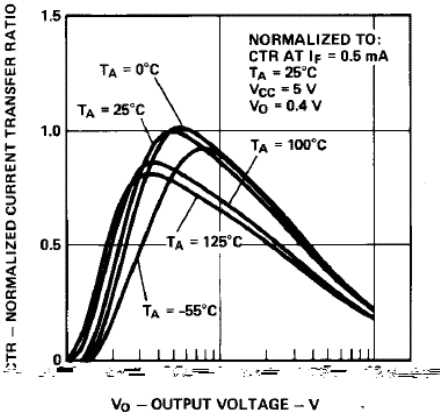


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

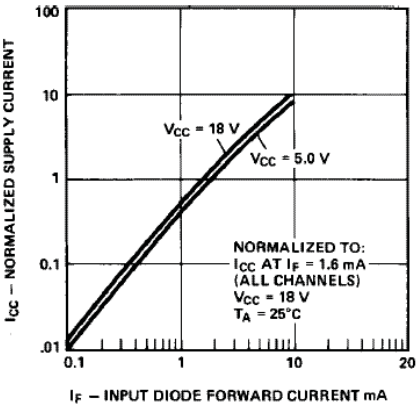


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

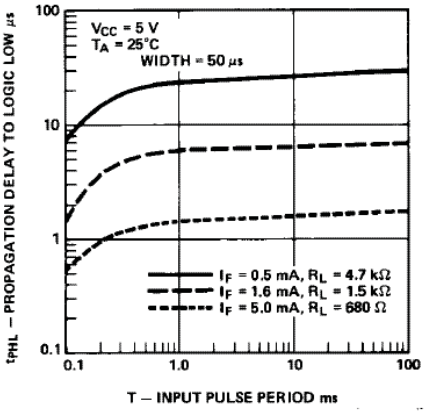


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

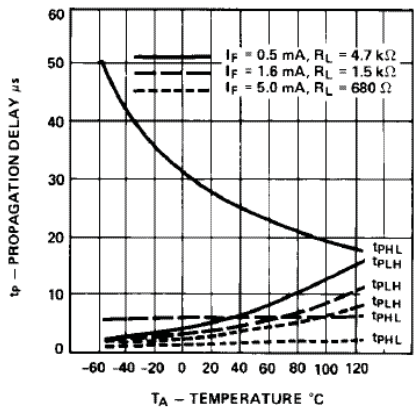


Figure 6. Propagation Delay vs. Temperature.

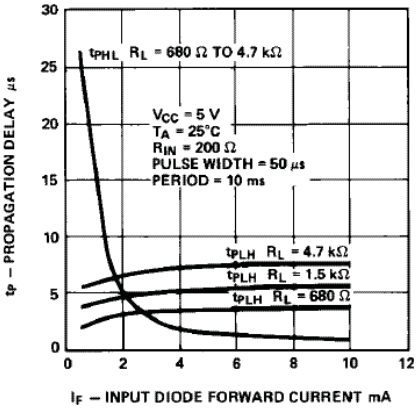
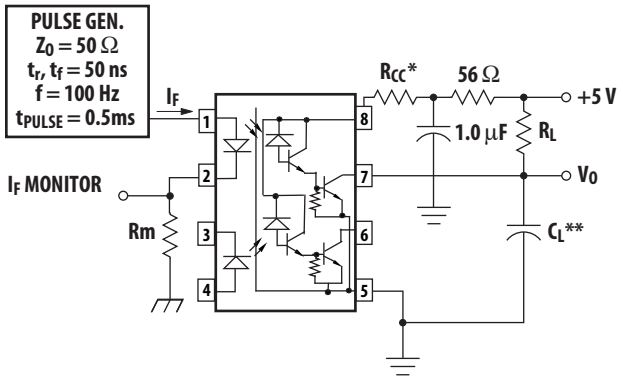


Figure 7. Propagation Delay vs. Input Diode Forward Current.



* SEE NOTE 11
** C_L INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

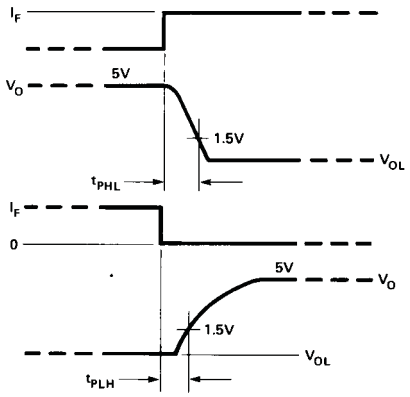
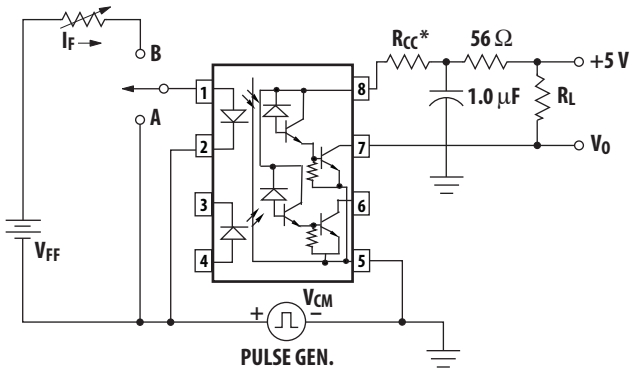


Figure 8. Switching Test Circuit (f, t_P not JEDEC registered).



* SEE NOTE 11

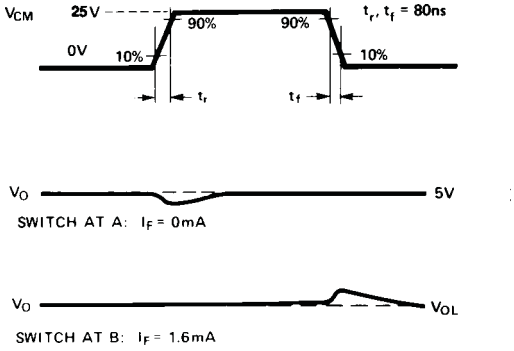


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

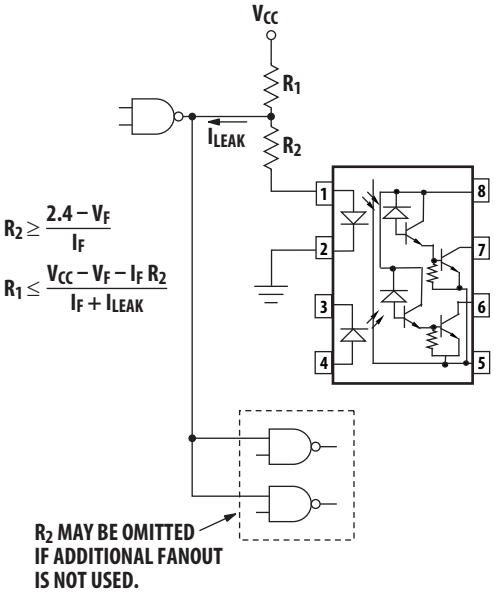
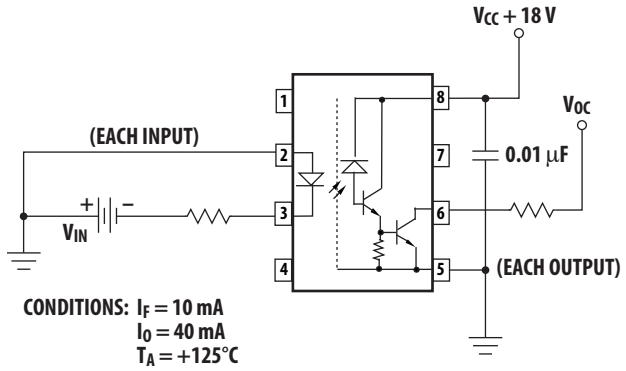


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

MIL-PRF-38534 Class H, Class K, and DLA SMD Test Program

Avago's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H and Class K devices are also in compliance with DLA drawings 83024, 5962-89785, 5962-89810, and 5962-98002.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.



*** ALL CHANNELS TESTED SIMULTANEOUSLY.**

Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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