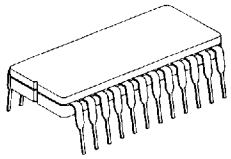
NMOS 128 x 8 BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

The EF 6810 is a byte-organized memory designed for use in bus organized systems. It is fabricated with N-channel silicon gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

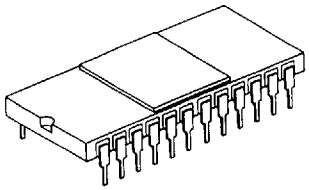
The memory is compatible with the 6800 Microcomputer family, providing random storage in byte increments. Memory expansion is provided through multiple Chip select inputs.



J Suffix
DIL 24
Ceramic Cerdip package
(preferred package)

MAIN FEATURES

- Organized as 128 bytes of 8 bits.
- Stactic operation.
- Bidirectional three-state data input/output.
- Six chip select inputs (four active low, two active high).
- Single 5-volt power supply.
- TTL compatible.
- Maximum access time = 450 ns – EF 6810
  360 ns – EF 68A10
  250 ns – EF 68B10.



C Suffix
DIL 24
Ceramic Side Brazed package
(on special request only)

See the ordering information page 11.

Pin connection : see page 11.

SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883C (class B).
- NFC 96883 class G.
- or according to TMS standards.

SUMMARY

A - GENERAL DESCRIPTION

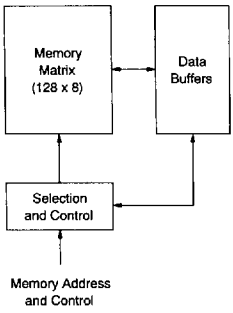


Figure 1.1 : EF 6810 random access memory block diagram.

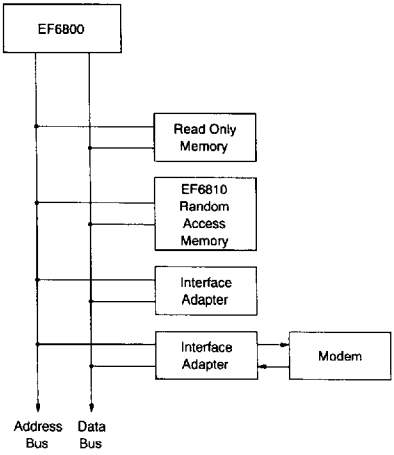


Figure 1.2 : EF 6800 microcomputer family block diagram.

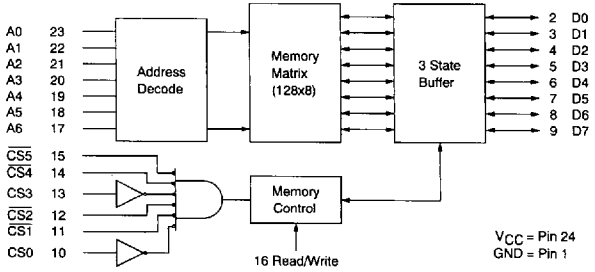


Figure 1.3 : Block diagram.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the SRAM EF 6810, in compliance with MIL-STD-883 class B Rev. B.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown § 9.1 page 11/12.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 24 leads DIL Ceramic Side Brazed
- 24 leads DIL Ceramic Cerdip.

The precise case outlines are described § 8 page 10/12.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter		Test conditions	Min	Max	Unit
V_{CC}	Supply voltage			−0.3	+7.0	V
V_I	Input voltage			−0.3	+7.0	V
P_{dmax}	Max Power dissipation		T_{case} = −55°C		0.55	W
			T_{case} = +125°C		0.4	W
T_{case}	Operating temperature	M suffix	f = 1 and 1.5 MHz	−55	+125	°C
		V suffix	f = 1 and 1.5 MHz	−40	+85	°C
		No suffix	f = 1, 1.5 and 2 MHz	0	+70	°C
T_{stg}	Storage temperature			−55	+150	°C
T_j	Junction temperature				+160	°C
T_{leads}	Lead temperature		Max 5 sec. soldering		+270	°C

Note : This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

3.4 - Thermal characteristics (at 25°C)

Table 2

Package	Symbol	Parameter	Value	Unit
DIL 24	θ JA	Thermal resistance - Ceramic junction to ambient	60	°C/W
Cerdip	θ JC	Thermal resistance - Ceramic junction to case	15	°C/W
DIL 24	θ JA	Thermal resistance - Ceramic junction to ambient	65	°C/W
Ceramic	θ JC	Thermal resistance - Ceramic junction to case	15	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output
Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 - Thomson logo
3.6.2 - Manufacturer's part number
3.6.3 - Class B identification
3.6.4 - Date-code of inspection lot
3.6.5 - ESD identifier if available
3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics are specified for inspection purpose, refer to relevant specification :
Table 3 : Static electrical characteristics for all electrical variants. See § 5.2.
Table 4 : Dynamic electrical characteristics See § 5.3.

For static characteristics, test methods refer to Table 3 and § 5.4 of this specification.

For dynamic characteristics (Tables 4 and 5), test methods refer to IEC 748-2 method number, where existing.

5.2 - Static characteristics

Table 3 - DC electrical characteristics

V_{CC} = 5.0 V_{dc} ±5 % ; V_{SS} = 0 ; T_c = −55°C / +125°C or −40°C / +85°C (unless otherwise noted)

Symbol	Characteristic	Typ	Max	Unit
V_{IH}	Input high voltage	V_{SS} +2.0	V_{CC}	V
V_{IL}	Input low voltage	V_{SS} −0.3	V_{SS} +0.8	V
I_{in}	Input current (A_n, R/$\overline{W}$, CS_n) (V_{in} = 0 to 5.25 V)		2.5	µA
V_{OH}	Output high voltage (I_{OL} = −205 µA)	2.4		V
V_{OL}	Output low voltage (I_{OL} = 1.6 mA)		0.4	V
I_{TSI}	Output leakage current (three-state) ($\overline{CS}_n$ = 0.8 V or $\overline{CS}_n$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)		±10	µA
I_{CC}	Supply current 1.0 MHz (V_{CC} = 5.25 V, all other pins grounded) 1.5, 2.0 MHz		80 100	mA mA
C_{in}	Input capacitance (A_n, R/$\overline{W}$, $\overline{CS}_n$) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		7.5	pF
C_{out}	Output capacitance (D_n) (V_{out} = 0, T_A = 25°C, f = 1.0 MHz, CSO = 0)		12.5	pF

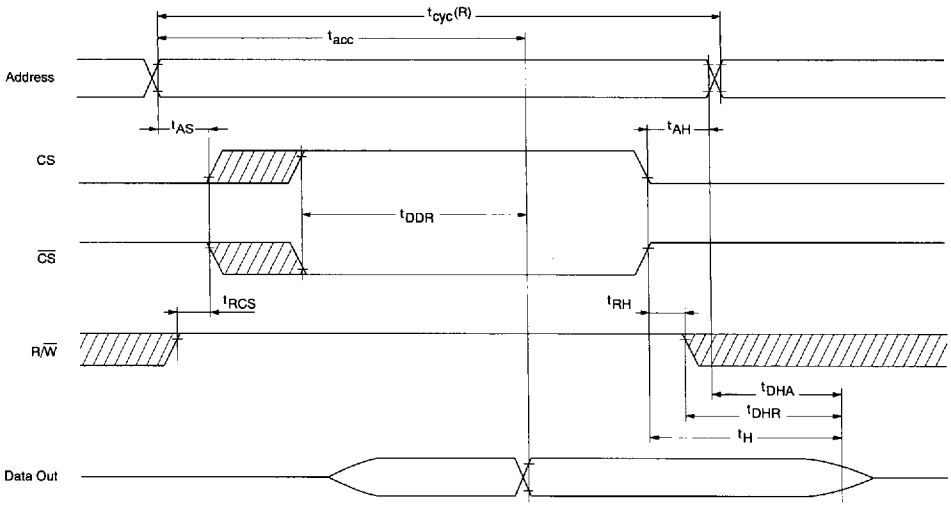
5.3 - Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.75 V to 5.25 V V_{IL} = 0.8 V and V_{IH} = 2.0 V.

Table 4 - AC operating conditions and characteristics

Read cycle V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 ; T_C = −55°C to +125°C (unless otherwise noted) - see Figure 2

Symbol	Characteristics	EF 6810		EF 68A10		EF 68B10		Unit
		Min	Max	Min	Max	Min	Max	
t_{cyc} (R)	Read cycle time	450		360		250		ns
t_{acc}	Access time		450		360		250	ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	0		0		0		ns
t_{DDR}	Data delay time (read)		230		220		180	ns
t_{RCS}	Read to select delay time	0		0		0		ns
t_{DHA}	Data hold from address	10		10		10		ns
t_H	Output hold time	10		10		10		ns
t_{DHR}	Data hold from read	10	80	10	60	10	60	ns
t_{RH}	Read hold from chip select	0		0		0		ns



Note 1 : Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
Note 2 : Measurement point shown are 0.8 V and 2.0 V, unless otherwise specified.
Note 3 : CS and CS have same timing.

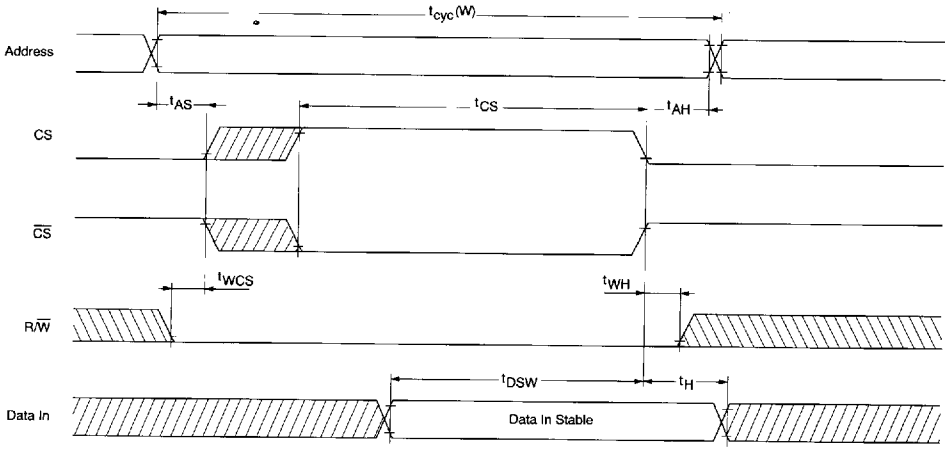
= Don't Care

Figure 2 : Read cycle timing.

Table 5 - AC operating conditions and characteristics

Write cycle V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 ; T_C = −55°C to +125°C (unless otherwise noted) - see Figure 3

Symbol	Characteristics	EF 6810		EF 68A10		EF 68B10		Unit
		Min	Max	Min	Max	Min	Max	
t_{cyc} (W)	Write cycle time	450		360		250		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	0		0		0		ns
t_{CS}	Chip select pulse width	300		250		210		ns
t_{WCS}	Write to chip select delay time	0		0		0		ns
t_{DSW}	Data setup time (write)	190		80		60		ns
t_H	Input hold time	10		10		10		ns
t_{WH}	Write hold time from chip select	0		0		0		ns



Note 1 : Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
Note 2 : Measurement point shown are 0.8 V and 2.0 V, unless otherwise specified.
Note 3 : CS and CS have same timing.

= Don't Care

Figure 3 : Write cycle timing.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

Figure here below shows the loading network applicable to the timing table.

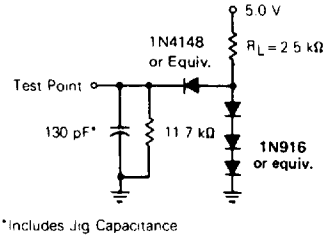


Figure 4 : AC test load.

6 - PREPARATION FOR DELIVERY

6.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

6.2 - Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with the different proposed norms and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

5

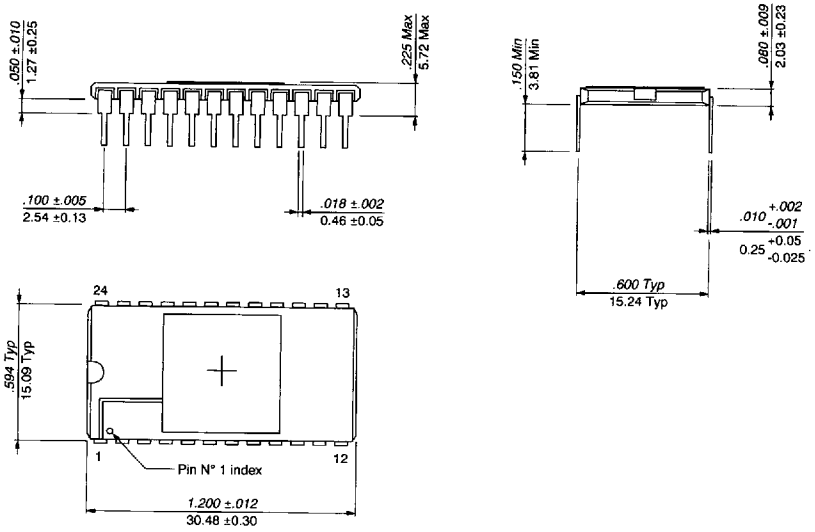
7 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

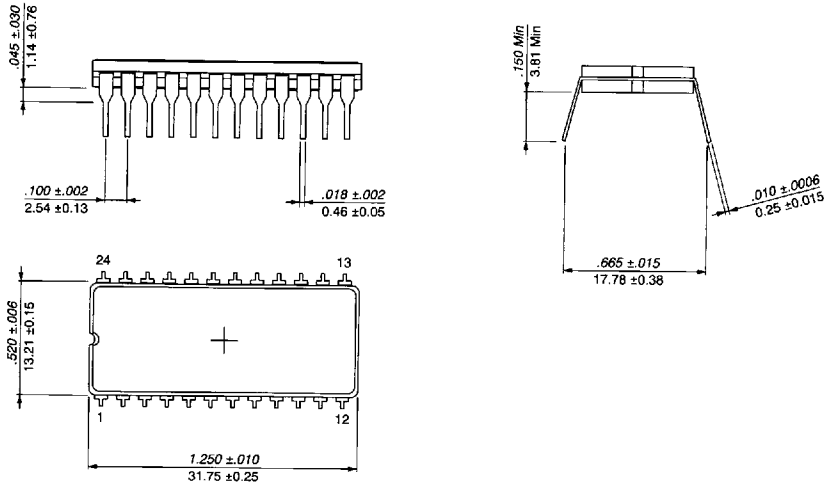
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

8 - PACKAGE MECHANICAL DATA

8.1 - 24 pins - DIL Ceramic Side Brazed

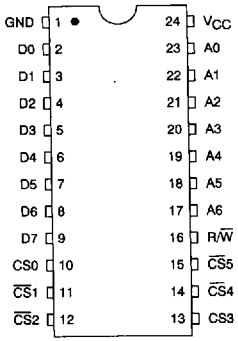


8.2 - 24 pins - DIL Ceramic Cerdip



9 - TERMINAL CONNECTIONS

9.1 - DIL 24 - pin assignments



10 - ORDERING INFORMATION

10.1 - Hi-REL product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6810JMG/B	NFC 96863 class G	DIL Cerdip	−55 / +125	1	Data sheet
EF6810CMG/B	NFC 96863 class G	DIL side Brazed	−55 / +125	1	Data sheet
EF68A10JMG/B	NFC 96863 class G	DIL Cerdip	−55 / +125	1.5	Data sheet
EF68A10CMG/B	NFC 96863 class G	DIL side Brazed	−55 / +125	1.5	Data sheet
EF6810JMB/B	MIL-STD-883 B class B	DIL Cerdip	−55 / +125	1	Data sheet
EF6810CMB/B	MIL-STD-883 B class B	DIL side Brazed	−55 / +125	1	Data sheet
EF68A10JMB/B	MIL-STD-883 B class B	DIL Cerdip	−55 / +125	1.5	Data sheet
EF68A10CMB/B	MIL-STD-883 B class B	DIL side Brazed	−55 / +125	1.5	Data sheet
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

Cerdip is preferred package.

11.2 · Standard product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6810CV	TMS Standard	DIL side brazed	−40 / +85	1	Data sheet
EF6810JV	TMS Standard	DIL cerdip	−40 / +85	1	Data sheet
EF68A10CV	TMS Standard	DIL side brazed	−40 / +85	1.5	Data sheet
EF68A10JV	TMS Standard	DIL cerdip	−40 / +85	1.5	Data sheet
EF6810JM	TMS Standard	DIL cerdip	−55 / +125	1	Data sheet
EF6810CM	TMS Standard	DIL side brazed	−55 / +125	1.5	Data sheet
EF68A10JM	TMS Standard	DIL cerdip	−55 / +125	1.5	Data sheet
EF68A10CM	TMS Standard	DIL side brazed	−55 / +125	1.5	Data sheet
EF6810C	TMS Standard	DIL side brazed	0 / +70	1	Data sheet
EF6810J	TMS Standard	DIL cerdip	0 / +70	1	Data sheet
EF68A10C	TMS Standard	DIL side brazed	0 / +70	1.5	Data sheet
EF68B10J	TMS Standard	DIL cerdip	0 / −70	2	Data sheet
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

Cerdip is preferred package.